FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
108339-00047	09/650,260
APPLICANT	
LIU et al.	
FILING DATE	GROUP
August 29, 2000	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
TL	AA	5,555,398	Sep. 10, 1996	Raman			Apr. 15, 1994
	AB	5,644,784	Jul. 1, 1997	Peek			Mar. 3, 1995
	AD	5,828,653	Oct. 27, 1998	Goss			Apr. 26, 1996
	AE	5,423,015	Jun. 6, 1995	Chung			May 21, 1991
	AF	5,696,899	Dec. 9, 1997	Kalwitz			Nov. 18, 1992
	AG	6,061,351	May 9, 2000	Erimli et al.			Dec. 18, 1997
	AH	5,748,631	May 5, 1998	Bergantino et al.			May 9, 1996
	AI	6,119,196	Sep. 12, 2000	Muller et al.			Jun. 30, 1997
	AJ	6,175,902 B1	Jan. 16, 2001	Runaldue et al.			Dec. 18, 1997
	AK	5,473,607	Dec. 5, 1995	Hausman et al.			Aug. 9, 1993
	AL	5,787,084	Jul. 28, 1998	Hoang et al.			Jun. 5, 1996
	AM	5,845,081	Dec. 1, 1998	Rangarajan et al.			Sep. 3, 1996
	AN	5,892,922	Apr. 6, 1999	Lorenz			Feb. 28, 1997
	AO	5,802,287	Sep. 1, 1998	Rostoker et al.			Aug. 3, 1995
	AP	6,011,795	Jan. 4, 2000	Varghese et al.			Mar. 20, 1997
	AQ	6,185,185 B1	Feb. 6, 2001	Bass et al.			Nov. 21, 1997
	AR	5,524,254	Jun. 4, 1996	Morgan et al.			Jul. 1, 1994
	AS	5,987,507	Nov. 16, 1999	Creedon et al.			Dec. 29, 1998
	AT	5,831,980	Nov. 3, 1998	Varma et al.			Sep. 13, 1996
	AU	5,781,549	Jul. 14, 1998	Dai			Feb. 23, 1996
	AV	6,041,053	Mar. 21, 2000	Douceur et al.			Sep. 18, 1997
	AW	5,459,717	Oct. 17, 1995	Mullan et al.			Mar. 25, 1994
	AX	5,909,686	Jun. 1, 1999	Muller et al.			Jun. 30, 1997
	AY	5,887,187	Mar. 23, 1999	Rostoker et al.			Apr. 14, 1997
	AZ	5,568,477	Oct. 22, 1996	Galand et al.			Jun. 27, 1995
	BA	5,414,704	May 9, 1995	Spinney			Apr. 5, 1994
	BB	5,390,173	Feb. 14, 1995	Spinney et al.			Oct. 22, 1992
	BC	5,825,772	Oct. 20, 1998	Dobbins et al.			Apr. 2, 1996
TL	BD	5,790,539	Aug. 4, 1998	Chao et al.			Jan. 29, 1996

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
TLL	BE	5,918,074	Jun 29, 1999	Wright et al.			Jul. 25, 1997
	BF	5,898,687	Apr. 27, 1999	Harriman et al.			Jul. 24, 1996
	BG	5,940,596	Aug. 17, 1999	Rajan et al.			Aug. 4, 1997
	BH	5,802,052	Sep. 1, 1998	Venkataraman			Jun. 26, 1996
	BI	5,842,038	Nov. 24, 1998	Williams et al.			Oct. 10, 1996
	BJ	5,742,613	Apr. 21, 1998	MacDonald			Apr. 27, 1993
	BK	5,579,301	Nov. 26, 1996	Ganson et al.			Feb. 28, 1994
	BL	5,278,789	Jan. 11, 1994	Inoue et al.			Dec. 6, 1991
	BM	5,652,579	Jul. 29, 1997	Yamada et al.			Aug. 15, 1996
TLL	BN	5,499,295	Mar. 12, 1996	Cooper			Aug. 31, 1993

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	NO	PART.
TLL	BO	WO9900936A1	Jun. 12, 2001	WIPO					
	BP	EP0465090A1	Jan. 8, 1992	EPO					
	BQ	EP0859492A2	Aug. 19, 1998	EPO					
	BR	EP0312917A2	Apr. 26, 1989	EPO					
	BS	EP0853441A2	Jul. 15, 1998	EPO					
	BT	4-189023	Jul. 7, 1992	Japan					Abs
	BU	WO 98/09473	Mar. 5, 1998	WIPO					
	BV	EP0752796A2	Jan. 8, 1997	EPO					
	BW	EP0862349A2	Sep. 2, 1998	EPO					Abs
	BX	FR 2 725 573 - A1	Apr. 12, 1996	France					Abs
	BY	EP0854606A2	Jul. 22, 1998	EPO					
	BZ	WO 99/00948	Jan. 7, 1999	WIPO					
	CA	WO 99/00949	Jan. 7, 1999	WIPO					
	CB	WO 99/00950	Jan. 7, 1999	WIPO					
	CC	WO 99/00939	Jan. 7, 1999	WIPO					
	CD	WO 99/00938	Jan. 7, 1999	WIPO					
	CE	WO 99/00944	Jan. 7, 1999	WIPO					
	CF	WO 99/00945	Jan. 7, 1999	WIPO					
	CG	EP0849917A2	Jun. 24, 1998	EPO					
TLL	CH	EP0907300A2	Apr. 7, 1999	EPO					

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)* Sheet 3 of 3

TLL	CI	"A High-Speed CMOS Circuit for 1.2-Gb/s 16 x 16 ATM Switching," Alain Chemarin et al. 8107 IEEE Journal of Solid-State Circuits 27(1992) July, No. 7, New York, US, pages 1116-1120
	CJ	"Local Area Network Switch Frame Lookup Technique for Increased Speed and Flexibility," 7001 IBM Technical Disclosure Bulletin 38(1995) July, No. 7, Armonk, NY, US, pages 221-222
	CK	"Queue Management for Shared Buffer and Shared Multi-buffer ATM Switches," Yu-Sheng Lin et al. Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C., March 24, 1996, pages 688-695
	CL	"A 622-Mb/s 8 x 8 ATM Switch Chip Set with Shared Multibuffer Architecture," Harufusa Kondoh et al., 8107 IEEE Journal of Solid-State Circuits 28(1993) July, No. 7, New York, US, pages 808-814
	CM	"Catalyst 8500 CSR Architecture," White Paper XP-002151999, Cisco Systems Inc. 1998, pages 1-19
TLL	CN	"Computer Networks," A.S. Tanenbaum, PRENTICE-HALL INT., USA, XP-002147300(1998), Sec. 5.2-Sec. 5.3, pages 309-320

EXAMINER	DATE CONSIDERED
	12/29/03

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.